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LTE Release 10 Small Cell Physical Layer Evolution *Issues and Challenges Facing Small Cell Product Developers in Multi-Core Environments*

By Brian Meads, Director of Software Sales, [CommAgility](http://www.commagility.com)

LTE Industry Trends, Drivers

Many studies, as well as current operator traffic trends, indicate massive growth in mobile traffic over the next few years. The oft-quoted Cisco VNI (Visual Networking Index) study shows mobile data traffic increasing from 885 PB/month in 2012 to 11,157 PB/month in 2017, a CAGR of 66%. Driver for this growth is generally accepted to be increased consumption, as well as creation and transmission of, multimedia content by wireless users.

While such growth puts tremendous pressure on the entire network from terminals to the core, this article will explore the challenges faced by Small Cell product developers, particularly in the development and deployment of the Physical Layer and the Protocol Stack. Small Cells are expected to bear much of the coverage and capacity burden in the Radio Access Network by 2017.

Small Cells share characteristics with both base stations and terminals. Clearly, they have to contain the functionality of macro cell base stations as well as other functionality that helps them co-exist with macro cells. However, similar to terminals, a lower price point than for macro cells is needed to enable deployment of large volumes. This requires a higher level of silicon and software integration, lower power consumption and a high level of interoperability testing. Power consumption becomes an issue for Small Cells – if products can be powered over Ethernet (PoE), the challenge of locating a Small Cell in proximity of a power source is reduced.

Just as the industry is getting over the teething pains of deploying Release 8 and 9-capable products, features in Release 10 are demanded to enable deployment of large numbers of small cells. For Small Cells, the key features in Release 10 are: Carrier Aggregation, Relaying, Coordinated Multi-Point, Enhanced Uplink/Downlink (UL/DL) Multiple Antenna Transmission (up to 8 antennas), Self Organizing Network Enhancements and Multimedia Broadcast Enhancements.

In particular, products supporting Release 10 require approximately 10x more GOPS than a Release 9 product. This requires a new generation of SoCs with new architectures that can deliver this processing power.

Multi-core SoCs, combining several DSP cores with multiple RISC processor cores, are at the center for Software Defined Radio deployment. The combination of DSP, RISC, accelerator cores are the only current architecture to support the needed GOPS and MIPS, while minimizing battery drain, required by 4G products.

Impact of Release 10 on eNodeB Processing Requirements

Two of the key features demanded by network operators have the most significant impact on the Physical Layer (PHY) software:

Carrier Aggregation – whereby two or up to five distinctly separate frequency bands are combined to create a single, virtual band to expand throughput. This effectively multiplies the performance to be delivered from the PHY. Simplest approach is to multiply cores and duplicate the PHY, which is not feasible, therefore requiring significant code optimization.

Enhanced Uplink/Downlink Multiple Antenna Transmission for LTE - Multiplies data rates through the use of up to 8 antennas (UL and/or DL). The increased throughput needs to be handled along with the corresponding encoding. This approximately doubles the performance required to handle inputs from the 8 antennas compared to Release 9.

Architecture Evolution – from 3GPP Release 9 to Release 10

In June 2011, Texas Instruments (TI) announced the TMS320TCI6614 SoC, which integrated quad C66 DSPs, an ARM Cortex A8 and layer 1 coprocessors and accelerators in single package for Small Cell product developers. The TCI6614 was among the first generation of LTE-capable SoCs introduced along with similar product from Mindspeed, Freescale and Cavium. Customers using this SoC were looking to address the outdoor pico- cell market – 64 active users, 2x2 MIMO, 20MHz Bandwidth, Cat 4 terminals (150Mbps DL / 50Mbps UL). These requirements are quite demanding compared to a home femto-cell supporting up to 8 or 16 active users.

Initial deployment of the PHY software was on a single C66 DSP core. This allowed for stabilization of initial functionality without adding the complexity of inter-core communication. As more and more complex test vectors were introduced, code profiling indicated candidate functions/modules for migrating to a separate core. Our testing methodology reflected the implementation sequence, grouped into White Box / Black Box categories. At Level 3.5, automated testing was added, to eliminate much of the manual test work and support regression testing.

White Box / Development Testing
<ul style="list-style-type: none"> • Level 1: Module Test • Level 2: Chain Test (LTE sub-frames) • Level 3: PHY Test (LTE frame)
Black Box / PHY IODT
<ul style="list-style-type: none"> • Level 3.5: PHY IODT against commercial test & measurement equipment

Table 1: PHY Testing Phases

Test vectors for PHY UL/DL were created using an internally developed C-code reference chain, which is a complete PHY implementation running non-real-time on a PC. Test Vectors include both end-points and intermediate points in the signal processing chain (white-box). They are then validated against an Agilent VSA. PHY testing is LTE sub-frame based and is executed on target.

Separate testing setups were used for Downlink and Uplink testing; Downlink setup is shown in Figure 1.

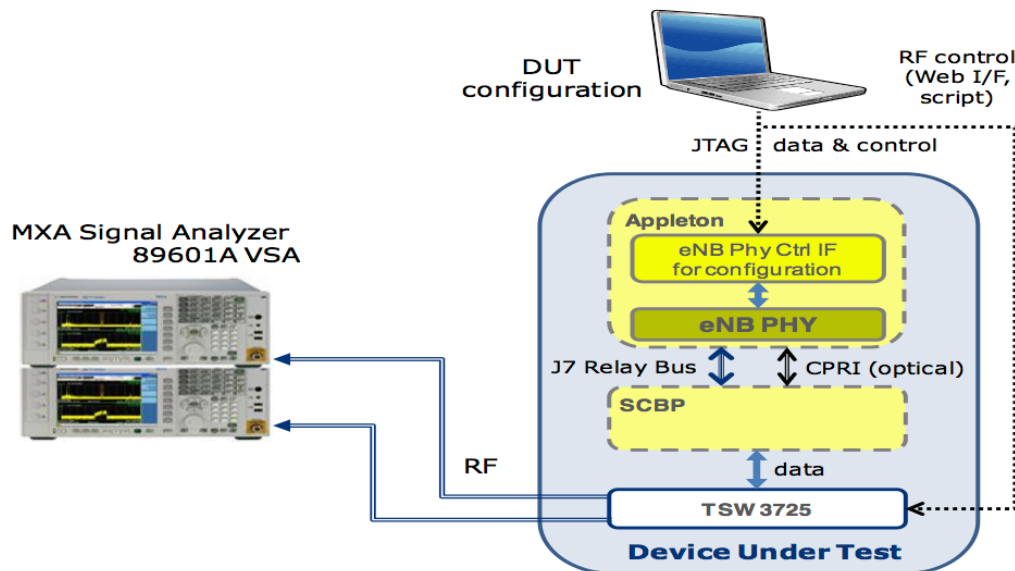


Figure 1: Downlink Testing Setup

As product maturity improved on the single core, the first victim to fall to the need for increased performance was the equalizer. Not surprisingly, it was the Equalizer that was shown to use up to 60% of a single C66 DSP. After the migration of the Equalizer was stabilized, the complexity of our testing increased, resulting in the migration of the Uplink De-multiplexer code to the same core with the Equalizer. At this point, full product requirements were met, so no further optimization was undertaken. This iterative, or Agile, methodology was seen as the most reliable path to achieve product quality release for customers.

Moving on to the requirements imposed by Release 10, there are multiple paths that SoC vendors can take to attain the approximate 10x performance improvement. Generally, these can be grouped into two main areas: 1) more/bigger cores and 2) increased clock/technology shrink.

Ultimately, Texas Instruments decided for a combination of increased number of cores along with moving from 40nm technology to 28nm. This approach is intended to maximize SoC performance while keeping risk and power consumption at a minimum. In addition, this new architecture opens the possibility for customers to develop multi-mode (3G and 4G) products on the same SoC.



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Clearly, the higher number of available DSP and RISC processors raises challenges to partitioning the software to achieve maximum performance. In addition, other elements of the SoC are stressed in new ways.

The most critical questions for the lead client are – what use cases need to be supported? What spectrum is available? What does the customer intend to integrate on the SoC beyond the core LTE functionality? This sets down the target requirements, and influences the architecture. For example, if both 3G and 4G are to be supported, this will determine how many cores (DSP or RISC) are available for the PHY as well as the Layers 2 and 3. The complete jump to full LTE-A is huge and must be addressed in a stepwise manner.

Evolution of the PHY software needs to proceed on the basis of the existing proven solution. Thus, the PHY will be migrated to the new SoC in the same configuration as the previous generation. As the integration is forthcoming over the next months, the results could be a subject of a subsequent article.

Nonetheless, the existing product becomes the new foundation to re-start the iterative process. Looking at this new architecture, several key areas have been identified to which particular attention will be paid.

The first step will be to revalidate the SoC/PHY software, running it through a series of regression tests to ensure that the robustness of the silicon and if any new bugs are exposed on the new SoC. The same test framework as described above will be used for this. New test vectors will be developed to stress test the sub-system beyond the capabilities of the first generation SoC.

Some elements have been enhanced in the new architecture, such as the Multicore Navigator, which facilitates inter-core communication. On top of the Multicore Navigator is the Navigator Runtime software package, which simplifies scheduling and load balancing. These enhancements need to be validated with the PHY software, perhaps leading to further optimization potential in the PHY.

The second step is to profile elements of the new architecture where performance improvements are expected. For example, an additional queue manager, which supports communication between cores or between a core and an accelerator, must be utilized. If not utilized, no gain can be derived.

The third level of testing involves maximizing the performance of the PHY software on the TCI6636 SoC. In this phase, addition of new features such as Carrier Aggregation and UL/DL Enhancements require the use of more DSP cores to take advantage of the potential performance increase.

Lastly, together with a lead customer, the 4G PHY is combined with a 3G PHY. At this point, all the critical sub-systems, inter-core communication, shared memory, DDR interfaces, the Multicore Navigator and more will be stressed to identify problem areas. The protocol stack is



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added, split across one of the C66 cores and an ARM A15. Shared memory and communication between the PHY and Stack is revalidated. This is seen as a potential system bottleneck.

Summary

Even though CommAgility has vast experience implementing Physical Layer software for LTE Small Cells and terminals, each new Software Defined Radio platform supported brings new lessons and knowledge. The keys for successful evolution are to 1) secure a solid, known foundation and 2) iteratively evolve the complexity. These are not new principles for software developers, but the depth and breadth of complexity introduced with each new generation of LTE standards quickly exposes those who are overconfident and too hasty to not adhere to these fundamentals in their attempts to be first to market.

About the Author

Brian Meads is Director of Software Sales at CommAgility. Active in the telecommunications industry for over twenty years, he has held commercial positions as head of Marketing at MCCI Corporation, Software Marketing Manager at Philips Semiconductors and Marketing Director at Lucent Microelectronics. Earlier engineering positions were at Optimay, GmbH, Siemens AG, Rohde & Schwarz and Magnavox, USA. His degrees are a BSEE from the University of Wisconsin-Madison and an MBA from EDHEC in Nice, France. He can be reached at brian.meads@commagility.com.

About CommAgility

CommAgility is a leading manufacturer of signal processing modules. Customers around the world use CommAgility products to develop high performance applications, with a particular focus on wireless baseband. CommAgility was honoured with a Queen's Award for International Trade in 2013, and has featured in the Deloitte UK Fast 50 list of fastest growing technology companies in 2012 and 2013.

In March 2015, CommAgility acquired MIMOon GmbH. As part of CommAgility, MIMOon's team will continue developing market leading physical layer and protocol stack software solutions for LTE eNodeB and UE product developers. The two company's products are now available from a single source, allowing customers to take the individual products or as integrated solutions.

We are agile and fast to react to our customers' specific needs, offering a base technology platform that we can quickly customise. We primarily work with OEM customers who we support closely in order to ensure success of their product.

CommAgility's engineering team is massively experienced, with the four co-founders each having worked in embedded signal processing for more than 20 years. The team has worked on cutting edge DSP and FPGA technology through multiple product generations, and has the expertise to develop systems quickly and effectively, and to deliver complicated projects on time, every time.