AMC-D24A4-RF2/RF4

DATASHEET

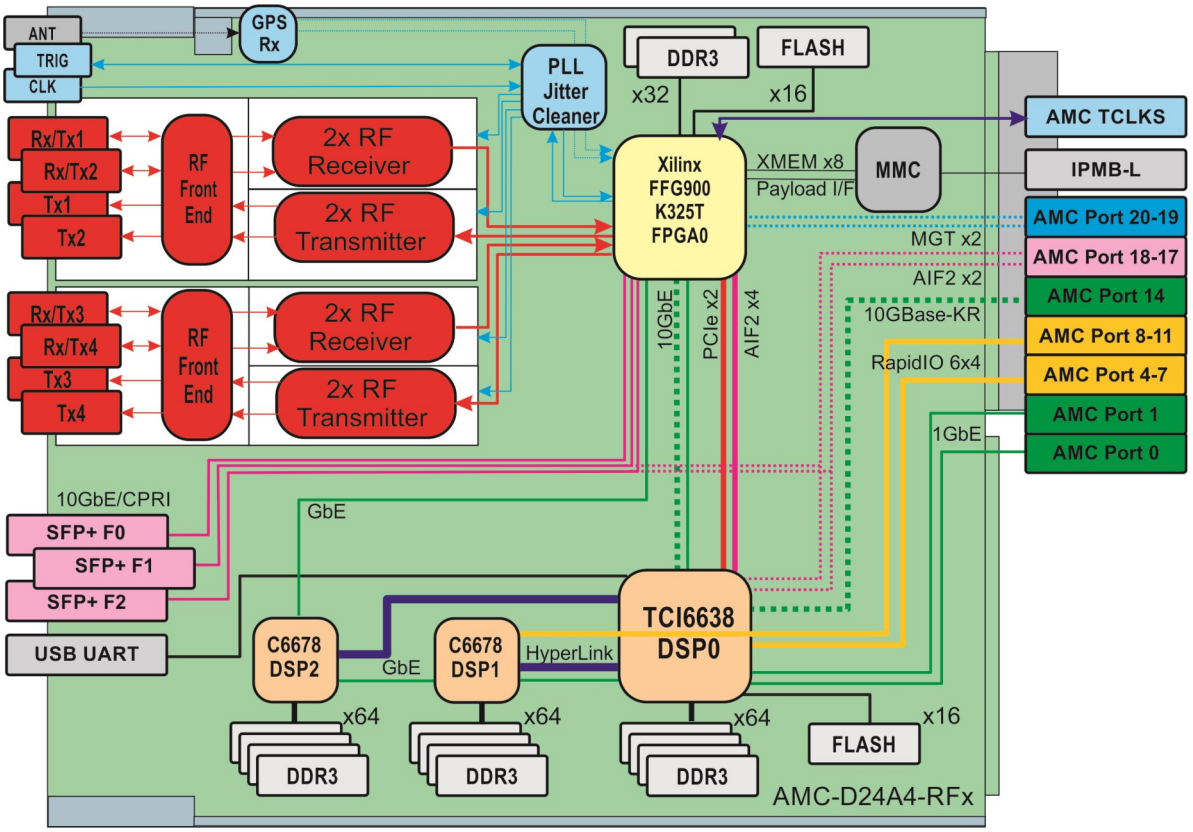
(for AMC-D24A4 non-RF variant, see page 4)

A highly integrated AdvancedMC card based on TI's TCI6638 and C6678 DSP SOCs, plus a large Xilinx Kintex-7 FPGA and 2x2 or 4x4 RF

Combines 4 ARM A15 cores with 24 C66x+ DSP cores, accelerators and shared memory, plus FPGA, RF and CPRI interfaces

Includes two or four high quality, flexible and wideband RF channels, supporting MIMO and carrier aggregation

Flexible, high bandwidth off-board communications via Gen2 Serial RapidIO and optional 10 GbE



The CommAgility AMC-D24A4 is an extremely high performance ARM, DSP and FPGA based processing card which includes integrated, flexible, wideband RF transceiver channels, all in the compact double width Advanced Mezzanine Card form factor. The AMC-D24A4-RF2 has two RF channels, while the AMC-D24A4-RF4 has four.

The module is aimed at LTE, LTE Advanced and 5G systems that require MIMO technologies, and enables complete RF to Layer 3 wireless basestation functionality to be implemented on a single card. The performance and flexibility is ideal for use in test equipment, research and development, or a specialized application such as wireless surveillance.

The module's main processor is the TMS320TCI6638, part of TI's new KeyStone II generation of DSP/ARM SoCs. It includes eight C66x+ DSP cores, as well as four ARM Cortex™-A15 cores for higher layer processing. Two additional TMS320C6678 octal C66x core DSPs maximize the AMC's processing capability, with all processors closely coupled through TI's Hyperlink interface and the Ethernet infrastructure of the card with Serial RapidIO (SRIO) backplane connectivity providing inter-card connectivity. There is also a large Kintex-7 FPGA for additional co-processing and to manage the RF interfaces. Kintex-7 provides an ideal compromise between size, speed and cost, and allows fitting of various FPGA sizes from K160T through to K410T.

CommAgility has ported the RF modules and capabilities of its existing AMC-RF2x2 card to the new module, keeping all the software configurable bandwidth (up to 40MHz+) and flexibility (662MHz to 3839MHz). With AMC-D24A4, it can now support 2 or 4 RF channels for 2x2 or 4x4 MIMO configurations, or alternatively on the AMC-D24A4-RF4, each pair of channels can be run at different frequencies, allowing carrier aggregation across different bands. The included RF control, management and processing firmware and software provides a high level RF control API while also leaving most of the board available for customer processing.

A comprehensive DSP Board Support Library is provided along with a full SMP Linux implementation for the ARM cores, for easy integration of 3rd party PHY, stacks and customer applications with the card.

Timing and synchronisation for applications is achieved with the built in GPS receiver, or via the front panel and AMC backplane clock I/O.

Texas Instruments Design Network

CommAgility Ltd
sales@commagility.com
www.commagility.com
Tel: +44 1509 228866

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AMC-D24A4-RF2/RF4

KEY FEATURES

- Full solution for RF through to SRIO, Gigabit or optional 10G Ethernet
- Two or four flexible, wideband RF ports
- Texas Instruments TMS320TCI6638 and TMS320C6678 DSP SoCs
- Large Xilinx Kintex-7 FPGA
- Full SMP Linux support for ARM cores configurable as a standard or real-time OS
- Comprehensive timing sync options plus 20 Gbaud backplane Serial RapidIO ports
- CPRI links to DSP (8x) or FPGA (16x); available without RF
- Double width Full Size PICMG AMC.0 R2.0 Advanced Mezzanine Card
- Can run "standalone" with just power and cooling

RESULTING BENEFITS

⇒ No other cards required for many systems, reducing system cost

⇒ Supports advanced Carrier Aggregation or 2x2/4x4 MIMO systems on single card

⇒ The latest high performance TI devices with a total of 24 DSP cores and 4 ARM cores, for advanced wireless applications

⇒ Supports custom acceleration and baseband processing alongside 10G CPRI links and CommAgility RF processing

⇒ Supports application, customer or 3rd party L2/L3 stacks and CommAgility RF and card control all running together

⇒ Allows high bandwidth connection and synchronisation of multiple cards for more complex systems such as 8x8 MIMO

⇒ Supports external Remote Radio Heads where on-board RF is not applicable

⇒ Works with industry standard MicroTCA chassis;

⇒ Minimal external hardware required for small applications, saving system cost

THE QUEEN'S AWARDS FOR ENTERPRISE: INNOVATION 2016

AdvancedMC™ µTCA® AdvancedTCA®

CommAgility Ltd, Loughborough, UK
Tel: +44 1509 228866

sales@commagility.com
www.commagility.com

AMC-D24A4-RFx

HARDWARE SPECIFICATIONS

DSP0: TMS320TCI6638 KeyStone II SoC:
- 8x C66x DSP cores @ 1.2 GHz
- 4x ARM A15 cores @ 1.4/1.2 GHz
- Accelerators and packet processors
- 2 Gbytes x64 DDR3-1600 SDRAM
- 256 Mbytes x16 boot FLASH
- 20 Gbaud, 4x SRIO V2.1 to backplane ports 4-7
- 10 Gbaud, 2x PCI Express link to FPGA
- 2x 40 Gbaud Hyperlink buses to DSP1, DSP2
- 4x 5 Gbaud AIF2 CPRI lanes to FPGA0
- Two AIF2 CPRI to backplane ports 18-17, or optional to front panel SFP+
- 5 port GbE switch with connections to DSP1, FPGA and two to backplane
- UART to front panel USB connector

DSP1, DSP2: TMS320C6678 each with:
- 8x C66x DSP cores @ 1.25 GHz
- 2 Gbytes x64 DDR3-1333 SDRAM
- 20 Gbaud, 4x SRIO V2.1 from DSP1 to backplane ports 8-11
- 40 Gbaud Hyperlink to DSP0
- GbE chained from DSP0, through DSP1 and DSP2, to FPGA0
- Optional 10 Gbaud, 2x PCI Express from DSP1 to backplane ports 4-5

FPGA0: Xilinx Kintex-7™ K325T-2 FPGA
- 1 Gbyte x32 DDR3-1600 SDRAM
- 256 Mbytes x16 FLASH; allows storage of multiple FPGA configuration images
- Gigabit Ethernet links to DSP0, DSP 2
- 10 Gbaud, 2x PCI Express to DSP0
- 3x MGT to front panel SFP+
- 2x MGT to AMC ports 20-19
- 4x 5 Gbaud CPRI to DSP0 AIF2

Timing:
- Integrated GPS for timing sync
- Front panel clock and sync
- AMC Telecom clock A-D support
- Configurable PLL/jitter cleaner

Front panel I/O:
- Two or four flexible RF channels, each with separate or combined Tx/Rx SMA ports
- 3x SFP+ to FPGA, up to 10.3 Gbaud
- 2x SFP+ to DSP AIF2 (build option)
- GPS aerial and 2 x SMB clock/sync
- USB UART for ARM configuration
- uTCA, DSP, FPGA, SFP+ and GPS LEDs

Form Factor and Backplane:
- Double-width, full-size Advanced Mezzanine Card, AMC.0 Rev 2.0 compliant
- Hot swap support
- AMC.4 compliant 20 Gbaud x4 SRIO to AMC ports 4-7 and 8-11
- AMC.2 compliant GigE to ports 0, 1
- FPGA MGT, DSP AIF2 to ports 20-17
- Chassis and logic ground bridged

Debug:
- Breakout board for debug and RS-232
- Separate FPGA JTAG debug connector
- RS-232 headers, LEDs for each DSP

Module Management Controller:
- AMC.0 IPMB_L, FRU EEPROM data
- Power & reset, health monitoring

RF SPECIFICATIONS

RF Channels:
- Two or four channels (in two sets of two)
- Each pair in a set is identical and frequency synchronized; the two sets can be synchronized or different frequencies
- Tx and Rx can be the same (TDD) or different (FDD) frequencies

Frequency and Bandwidth:
- RF Freq Range: 662 – 3839MHz
- RF Fine Freq Resolution: <1Hz
- RF Bandwidths supported: 1.4, 3, 5, 10, 15, 20, 40+ MHz
- Actual baseband sampling rates: Rx 122.88 MSPS, Tx 61.44 MSPS

Front End Modes:
- Separate Tx and Rx (FDD)
- Combined Tx/Rx (FDD)
- Switched Tx/Rx (TDD)
- Loopback Tx to Rx (calibration)

TX Ports:
- Maximum Tx power: +10dBm (CW)
- Tx Dynamic Range: >60dB
- EVM: <1.2% up to 3GHz; <2% higher (20MHz BW, Pout <0dBm)
- Power sensor range: -50dBm to 0dBm
- Power sensor accuracy (FDD, TDD2): ±0.5dB from –40dBm to 0dBm
- DAC SFDR: >70dB

RX Ports:
- Maximum input power (OFDM): +4dBm (normal operation) +30dBm (safety maximum)
- Gain range: 60dB
- EVM: <2% up to 3GHz; <3% higher (20MHz BW, +4dBm > Pin > -57dBm)
- Power sensor range: -50dBm to 0dBm
- Power sensor accuracy (FDD): ±1.5dB from –40dBm to 0dBm

Calibration and tuning:
- Power sensors factory calibrated over multiple power levels and frequencies
- Other RF parameters auto-tuned and cached in non-volatile storage

ENVIRONMENT/EMC/SAFETY
- Operating temp: 0-40°C ambient
- Power consumption: up to 86W max
- Designed for NEBS/ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2011/65/EU RoHS, 2012/19/EU WEEE and 2006/95/EC LVD compliant

SOFTWARE
Management: Full embedded suite based on Pigeon Point™ Software

FPGA: Xilinx Vivado project to show functionality; RF control and processing

DSP: TI RTOS Kernel BSP and drivers

ARM: Linux BSP and drivers; RF control

LTE PHY: SmallCellPHY-TI available fully integrated and tested with this product, minimising customer development work.

Contact CommAgility for further details of software and other stack partners.

OEM PARTNERSHIP SERVICES:

IN DEVELOPMENT: Support and training; hardware customisation; software and FPGA development.

IN PRODUCTION: lead-time reduction; extended warranty; and repair; quick turn repairs and/or spares stocking.

EXTENDED LIFE: obsolescence management; guaranteed lifecycle; Escrow.

LICENSING can be offered for high volume projects.

CommAgility

AMC-D24A4

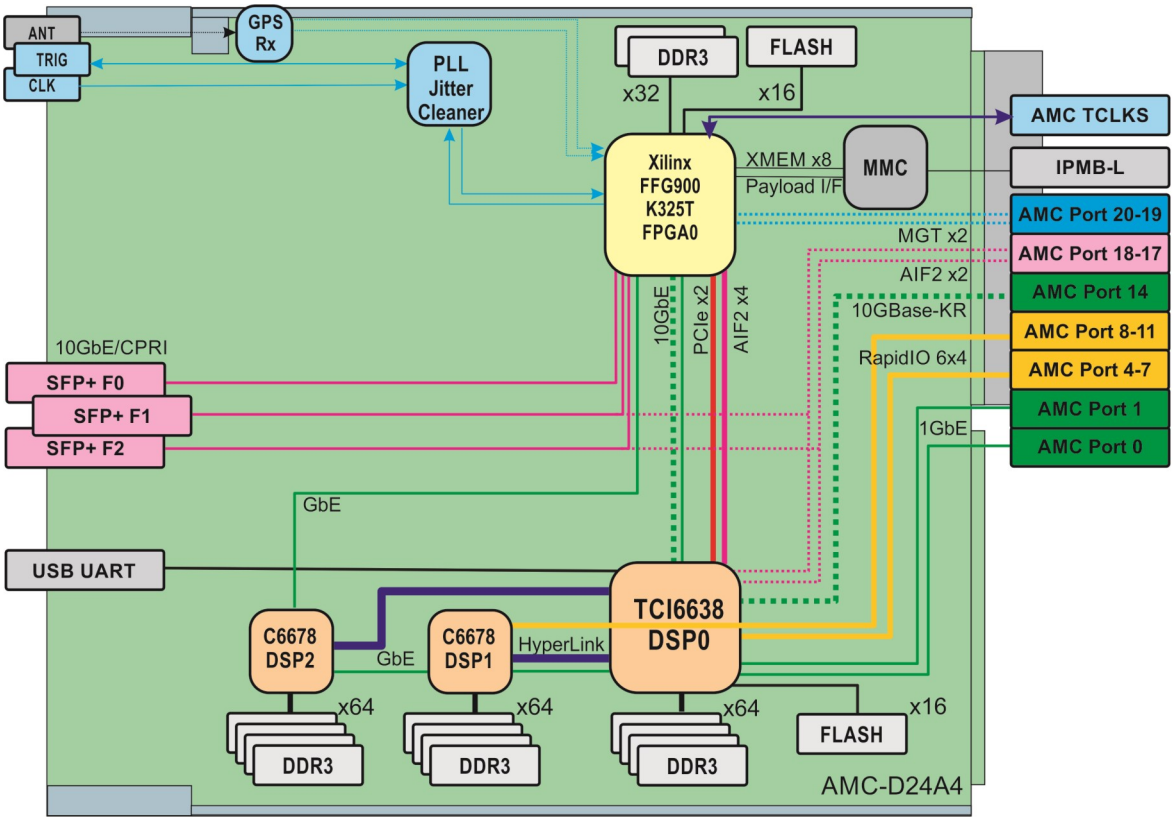
DATASHEET

A high performance AMC card based on a TI's TCI6638 and TMS320C6678 DSPs, plus a large Xilinx Kintex-7 FPGA

Combines 4 ARM A15 cores, 24 C66x+ DSP cores, accelerators and shared memory, with FPGA resource and CPRI interfaces

Flexible, high band-width off-board communications via Gen2 Serial RapidIO and optional 10 GbE

Three SFP+ to the front panel for CPRI or 10GbE, plus GPS and clock sync



The CommAgility AMC-D24A4 is an alternative solution to AMC-D24A4-RF4/RF2 when the on-board RF capability is not required, for example when external remote radio heads are being used in a larger base station or Cloud RAN architecture. The high performance ARM, DSP and FPGA based processing architecture remains the same, with up to 3 off-board 9.8 Gbaud 16x CPRI connections available from the FPGA as standard, or two 4.9 Gbaud 8x CPRI connections from the main DSP as a build option. A range of backplane connections for I/O expansion or connecting multiple cards are available, as well as 10GbE support to the front panel and backplane.

The AMC-D24A4 is a double-width AMC card, available as either mid-size or full-size to suit customer requirements.

HARDWARE SPECIFICATIONS

DSP0: TMS320TCI6638 KeyStone II SoC
DSP1, DSP2: TMS320C6678 SoC
FPGA0: Xilinx Kintex-7™ K325T-2 FPGA

- All details as AMC-D24A4-RF4/RF2

Timing:

- GPS, front panel and AMC clocking with PLL/jitter cleaner, as AMC-D24A4-RF4/RF2

Front panel I/O:

- 3x SFP+ to FPGA, up to 10.3 Gbaud
- 2x SFP+ to DSP AIF2 (build option)
- GPS aerial and 2 x SMB clock/sync
- USB UART for ARM configuration
- uTCA, DSP, FPGA, SFP+ and GPS LEDs

Form Factor, Backplane, Debug, MMC:

- Double-width, full-size or mid-size Advanced Mezzanine Card
- Otherwise as AMC-D24A4-RF4/RF2

ENVIRONMENT/EMC/SAFETY

- Operating temp: 0-40°C ambient
- Power consumption: up to 64W max
- Designed for NEBS/ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2011/65/EU RoHS, 2012/19/EU WEEE and 2006/95/EC LVD compliant

SOFTWARE

ARM, DSP, FPGA, Management:

- As AMC-D24A4-RF4/RF2, less RF control and processing
- Fully open for customer programming.

LTE PHY: SmallCellPHY-TI is available fully integrated and tested with this product, minimising customer development work

Contact CommAgility for further details of software partners.

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Xilinx Alliance Program

CommAgility Ltd
sales@commagility.com
www.commagility.com
Tel: +44 1509 228866

CommAgility