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LTE applications and OpenVPX

By Paul Moakes, technical director, [CommAgility](http://www.commagility.com)

Next Generation Technologies for Secure Comms

Reliable communications are critical in defense applications, and the ability to set up ad hoc networks where existing communications are absent or damaged is key to future combat systems.

When assessing the next generation of technology with which to upgrade existing military communications infrastructure, it's difficult to ignore standards-based solutions such as Long-Term Evolution (LTE) systems. These standards are developing at such a pace that their data transfer performance is already an order of magnitude greater than that of technologies developed purely for tactical communications, such as the [Joint Tactical Radio System \(JTRS\)](#).

Since LTE uses Internet Protocol (IP) for data transmission, radio security can be achieved from packet encryption technologies rather than developing a secure radio network, such as the Wideband Networking Waveform (WNW) used by the [JTRS](#).

And the widespread deployment of civilian LTE networks means a proliferation of field hardened LTE solutions. With that background, the appetite for developing a proprietary military radio network has gone and JTRS was terminated.

OpenVPX for COTS

LTE is a mature technology, and a large selection of commercial off-the-shelf (COTS) solutions already exists for base stations, user equipment (UE), and wireless test. It makes sense, then, that a move to LTE-based networks is also accompanied by a move to COTS-based solutions.

The ruggedized requirements for military systems require open standards COTS architecture that is up to the task. OpenVPX (VITA 65.0) is a widely adopted VPX-based standard which builds on the great success VME systems have had in this arena. The VPX-REDI specifications of VITA 48.0, with conduction-cooled and air-cooled versions, provide the assurance of mechanical ruggedization in COTS based military systems. These specifications also [deliver](#) on Size, Weight, and Power (SWaP) limits.

Being an open standard, component cards are available from an ecosystem of suppliers. This helps multi-sourcing, and means that a range of chassis architectures is available to suit different deployed scales and architectures. For example, developments can begin on the bench with 6-slot air-cooled systems and then migrate to 12-slot 19" rack equipment or conduction-cooled ATR solutions while using the same plug-in card architectures.

Ruggedizing COTS Solutions

One of the major challenges in supporting the VPX-REDI specification is the move from field-proved non-rugged systems to the OpenVPX conduction-cooled architecture. This is one of the challenges we are addressing today.

For example, the CommAgility AMC-D24A4-RF4 is a double-width AdvancedMC card comprising a wireless baseband processing carrier card and RF mezzanines. Aimed at the LTE and LTE-Advanced wireless test market, but also finding use in small captive base stations, this architecture is a great fit for rapidly deployable military communications.

Our task was to adapt this card for rugged VPX deployment. By looking at the design issues faced, and the choices made, we can explore the challenges faced by any COTS manufacturer in bringing LTE to VPX, and the factors that a customer should consider when reviewing vendors' products.

Mechanical Challenges

The first challenge addressed has been the creation of a VPX-REDI baseband processing card, the CommAgility VPX-D16A4. The VPX height profile limits the use of mezzanine-based solutions where power dissipation is high, and in this case led to the architecture being laid out on a single baseboard. This was achieved by making use of an increased Side 2 height profile in comparison to AdvancedMCs, thus allowing memory devices to be placed on Side 2. The VPX specification also supports the use of PCBs with more layers, which makes device fan-out easier and supports a higher density of components on Side 1.

The next task was the conduction cooling clamshell design that could achieve the required -40°C to +85°C operational range. Fortunately, the maturity of the VPX standards means that component parts, such as the card guides, of a conduction-cooled solution were readily available off the shelf. A custom heatsink could then be created based on thermal profiling of the card and incorporating the card guides.

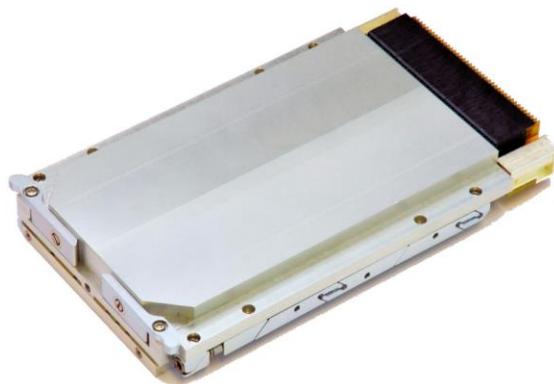


Figure 1: CommAgility VPX-D16A4

Backplane Mapping

Backplane mapping within the OpenVPX chassis is also important. Although governed by a set of pre-determined slot profiles within the specification, a wide variety of backplane architectures have been implemented. A base backplane configuration was identified, with the 2F2U configuration of a pair of ultra-thin control pipes and two fat pipes for fabric connection.

The VPX-D16A4 supports build options for both RapidIO fabric connectivity and PCIe connectivity. This is required to address the two main architectures supported by the card. RapidIO is required for its low latency in wireless applications where digital radio data is being transported on the backplane. However, PCIe is important where the digital radio data is being generated by the baseband card from Layer 3 data provided by a general-purpose processor card in the system, typically using an Intel device where RapidIO is not natively supported.

Payload Slot Profile SLT3-PAY-2F2U-14.2.3						
	ROW	OpenVPX	VPX-D16A4 3U	VPX-D16A4-PCIe	Profile	
J1	1	Data Plane Fat Pipe 0	SRIO 4x Gen2.1	PCIe 2x Gen2	Data Plane DP01	
	2					
	3					
	4					
	5	Data Plane Fat Pipe 1	SRIO 4x Gen2.1	PCIe 2x Gen2	Data Plane DP02	
	6					
	7					
	8					
	9	Data Plane Fat Pipe 2	FPGA GTX	FPGA GTX	User Defined (RTM/Expansion Plane)	
	10		FPGA GTX	FPGA GTX		
	11		DSP0 AIF2	DSP0 AIF2		
	12		DSP0 AIF2	DSP0 AIF2		
	13	Data Plane Fat Pipe 3	FPGA GTX	FPGA GTX		
	14		DSP0 XFI	DSP0 XFI		
	15		1000Base-BX	1000Base-BX		Control Plane CPutp02
	16		1000Base-BX	1000Base-BX		Control Plane CPutp01
J2	1	Expansion Plane 32 Pairs	FPGA LVDS x2	FPGA LVDS x2	User Defined (RTM/Expansion Plane)	
	2		FPGA LVDS x2	FPGA LVDS x2		
	3		FPGA LVDS x2	FPGA LVDS x2		
	4		FPGA LVDS x2	FPGA LVDS x2		
	5		FPGA LVDS x2	FPGA LVDS x2		
	6		FPGA LVDS x2	FPGA LVDS x2		
	7		FPGA LVDS x2	FPGA LVDS x2		
	8		FPGA LVDS x2	FPGA LVDS x2		
	9		FPGA LVDS x2	FPGA LVDS x2		
	10		FPGA LVDS x2	FPGA LVDS x2		
	11		FPGA LVDS x2	FPGA LVDS x2		
	12		FPGA LVDS x2	FPGA LVDS x2		
	13		FPGA LVDS x2	FPGA LVDS x2		
	14		FPGA LVDS x2	FPGA LVDS x2		
	15		FPGA LVDS/Clock x2	FPGA LVDS/Clock x2		
	16		FPGA LVDS/Clock x2	FPGA LVDS/Clock x2		

Figure 2: VPX-D16A4 Slot Profile

The user defined areas of the P1 connector were then allocated for high-speed point-to-point wireless communication with an RF card in the same chassis, or potentially a custom rear transition module (RTM). The DSPs supports CPRI direct connection to these ports from its antenna interface (AIF).

The FPGA supports P1 user defined connections to its high-speed transceivers. These transceivers are also capable of implementing a CPRI interface, but can additionally support the JESD204B protocol now widely being deployed as an interface for data converters. As well as supporting JESD204B, the P2 connector has been defined to support RF processing cards supporting a LVDS data interface. Usually this is implemented as a synchronous DDR interface, with the clocks provided with the data bus.

Support for a 10Gb Ethernet interface direct from the ARM-enabled DSP is provided by a native XFI interface. Where the baseband card is processing Layer 3 wireless data, 10Gb Ethernet is an important data path for wireless backhaul.

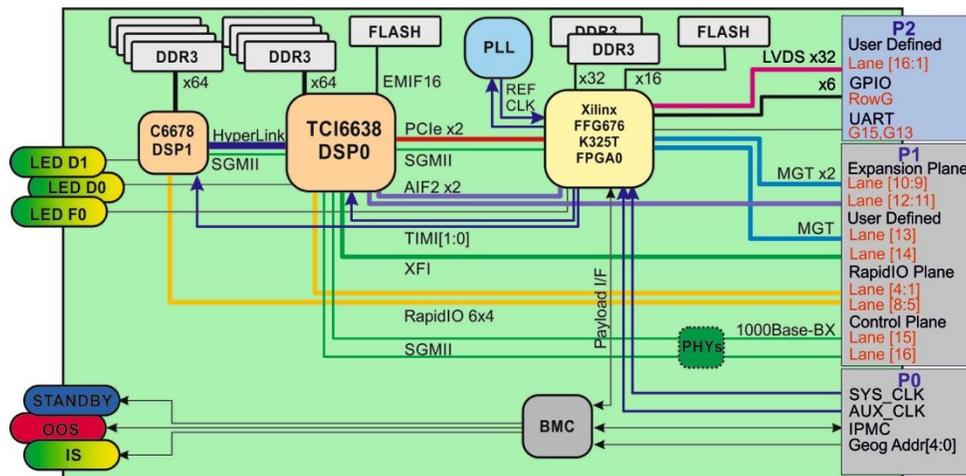


Figure 3: CommAgility VPX-D16A4 Block Diagram

Towards An RF Front End

The VPX-D16A4 is shipping to customers today. The next challenge we are addressing is the integration of an RF front end into the same ruggedized VPX chassis. Let's examine some of the issues around such an integration, and some possible solutions.

Digital Backplane Connectivity

To add an RF front end to the solution requires support for the necessary digital wireless bandwidth to the baseband card, determined by a combination of antenna diversity and data bandwidth. Higher bandwidths may dictate a JESD204B interface solution on the wireless transceiver rather than LVDS. Since the RF card is designed to act in tandem with the baseband card the backplane connectivity should be complementary.

Backplane architectures could support JESD204B or LVDS natively between the wireless transceivers and the baseband card. More generally however a local FPGA is used for flexible connectivity allowing additional low latency interconnects such as RapidIO to be used. The VPX-D16A4, for example, supports two 20Gbps RapidIO fat pipes, which can also be used to connect to an RF card.

The RF card must also support control of the RF transceivers, including channel switching for time-division duplex solutions, and handling the digital up and digital down conversion (DUC/DDC) required to support multiple sub-channels in the RF channel. This role usually falls to an FPGA device acting as a control processor which then also needs to be connected to the VPX control plane for card management.

RF Backplane Connectivity

Having defined an approach to support digital radio data transport across the backplane, a method is required to transport the analog RF data from the card to an external chassis interface.

Air cooled solutions can use a traditional front panel RF connector on an OpenVPX card, with a cabled solution from the chassis to the enclosure panel. Mounting the chassis with the front panel towards the rear of the enclosure allows the cabling to be kept neatly out of the way. However, this is not conducive to servicing the cards, which requires a re-cabling of the enclosure and can't be supported by conduction-cooled solutions.

This is one of the reasons VITA 67.0 has been developed. By supporting backplane co-axial connectivity front cards can be quickly swapped in and out of the chassis and there is no reliance on front panel IO in a conduction cooled environment. Using semi-rigid cabling from the analog RF section of the card to the VITA 67.0 connectors minimizes the RF loss and noise on the card.

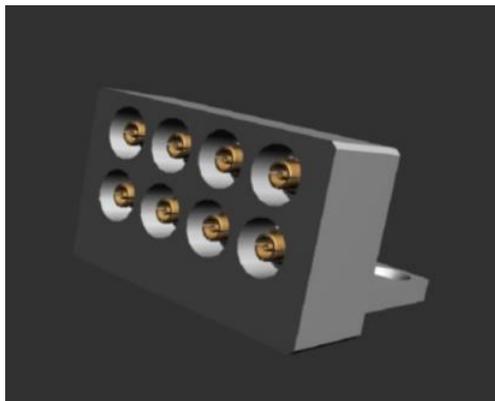


Figure 4: VITA 67.2 Connector. Image taken from VITA 67.0 specification.



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Conclusions

As military comms and secure radio applications continue to adopt commercial radio standards for the air interface, there exists an opportunity for COTS-based platforms developed for the commercial world to migrate to more ruggedized platforms. This is not without its challenges. Conduction cooling and SWaP consideration place additional constraints on equipment originally designed for the central office environment.

However, OpenVPX is an ideal platform on which to achieve this. It has a mature base standard with an ecosystem of off-the shelf building blocks, yet is flexible enough to introduce innovations such as backplane co-axial interconnect to address real-world problems. This combination of field proven technology and foresight make OpenVPX a standard with a future.

About the author

Paul Moakes PhD CEng MIET is technical director at CommAgility. He has previously held positions at Motorola and Blue Wave Systems. He is co-inventor of two patents in the field of MicroTCA and AdvancedMC. He holds a PhD in Electrical and Electronic Engineering from Sheffield University and a 1st Class Honours degree in Electronic Communications and Computer Systems Engineering from Bradford University.

About CommAgility

CommAgility is a leading manufacturer of signal processing AMC modules. Customers around the world use CommAgility products to develop high performance applications, with a particular focus on wireless baseband. CommAgility was honoured with a Queen's Award for International Trade in 2013, and has featured in the Deloitte UK Fast 50 list of fastest growing technology companies in 2012 and 2013.

We are agile and fast to react to our customers' specific needs, offering a base technology platform that we can quickly customise. We primarily work with OEM customers who we support closely in order to ensure success of their product.

CommAgility's engineering team is massively experienced, with the four co-founders each having worked in embedded signal processing for more than 20 years. The team has worked on cutting edge DSP and FPGA technology through multiple product generations, and has the expertise to develop systems quickly and effectively, and to deliver complicated projects on time, every time.