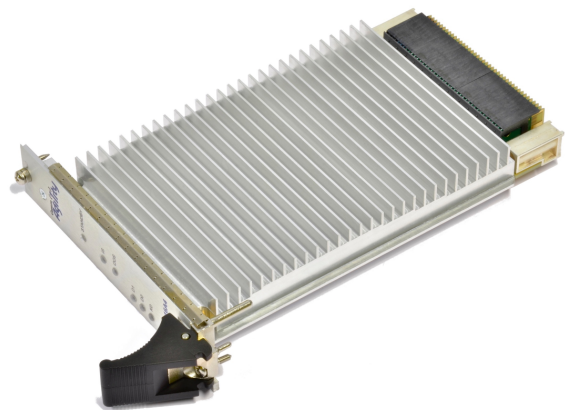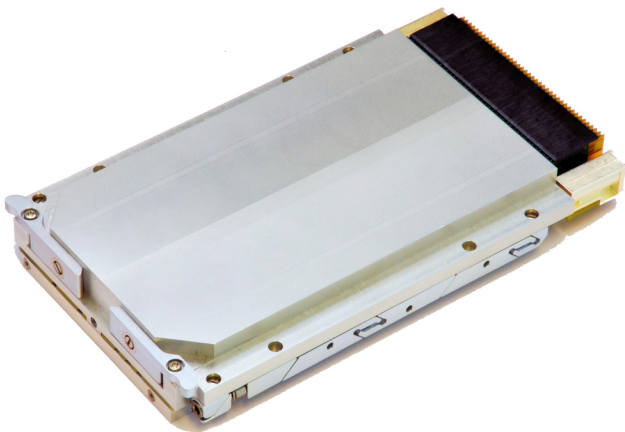# DATASHEET

VPX-D16A4-SRIO
High performance ARM, DSP and FPGA based processing module

- State of the art ARM/DSP/FPGA module based on the latest Texas Instruments and Xilinx devices
- 3U OpenVPX card supporting SRIO, Ethernet, CPRI and MGT to backplane plus links to RF or analog I/O
- Rugged VPX-REDI compliant design, available as either conduction cooled or air cooled
- Full Linux BSP and example software support covering Linux, multicore DSP and FPGA co-processing
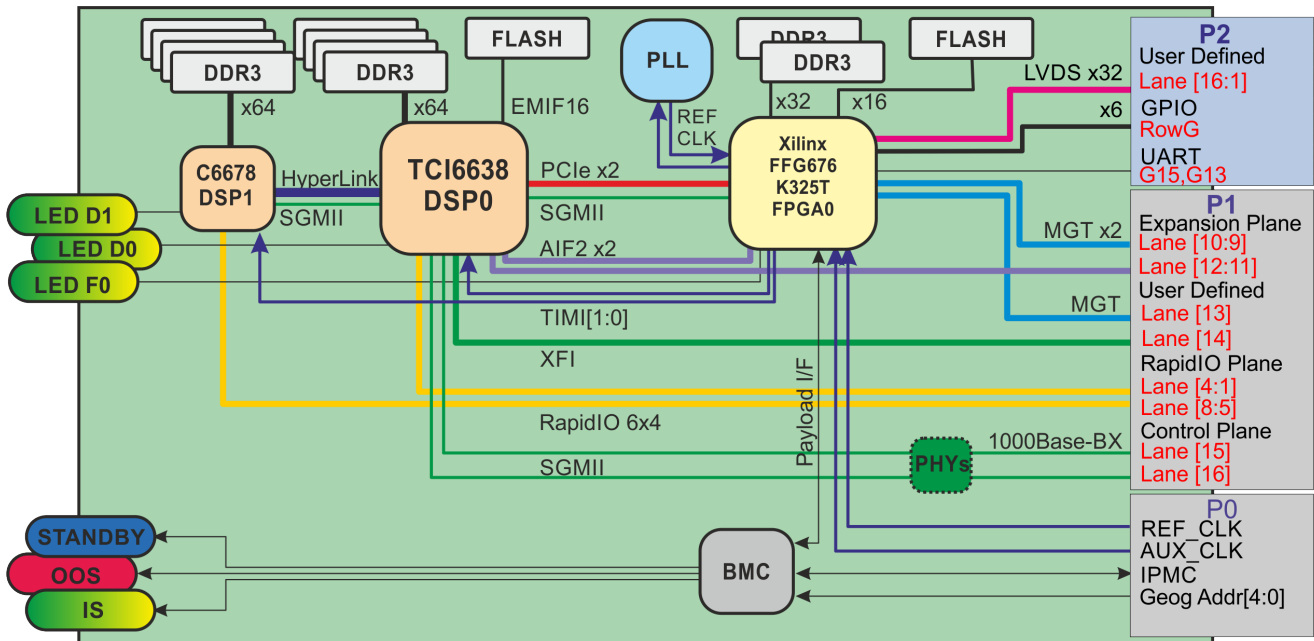
The VPX-D16A4-SRIO is a rugged high performance DSP/FPGA card in the compact VITA 65, 3U OpenVPX form factor. It is ideal for applications such as EW, SW radio, imaging or radar in harsh field deployment environments.

The card features 4x ARM A15 cores, 16x C66x+ DSP cores and various accelerators across two TI Keystone SoCs, each with its own large DDR3 memory bank and a 20Gbaud SRIO link to the VPX backplane. They are closely coupled with the Hyper-Link bus.

The main DSP is connected via PCI Express and AIF2 CPRI interfaces to a Xilinx Kintex-7 K325T FPGA, which has its own backplane

MGT, LDVS, GPIO and serial ports and a flexible clock generation PLL, enabling specialised I/O such as multi- channel RF or high speed ADC/DAC interfaces. All devices are also connected with Gigabit Ethernet.

A full Linux BSP and example software support is provided to accelerate customer development, based on TI's Linux and Multicore Software Development Kit and the Xilinx Vivado FPGA development suite. In addition, CommAgility's field proven LTE PHY software is available integrated with the card, with various options for L2/L3 software stacks.

DDR3 x64 **DDR3** x64 **FLASH** EMIF16 **PLL** REF CLK **DDR3** x32 **FLASH** x16 LVDS x32

C6678 DSP1 HyperLink SGMII
TCI6638 DSP0 PCIe x2 SGMII AIF2 x2
Xilinx FFG676 K325T FPGA0

LED D1 LED D0 LED F0

TIMI[1:0]
XFI
RapidIO 6x4
SGMII

x6 MGT x2 MGT 1000Base-BX PHYs

STANDBY OOS IS

Payload I/F BMC

P2
User Defined — Lane [16:1]
GPIO — RowG
UART — G15,G13

P1
Expansion Plane — Lane [10:9] / Lane [12:11]
User Defined — Lane [13] / Lane [14]
RapidIO Plane — Lane [4:1] / Lane [8:5]
Control Plane — Lane [15] / Lane [16]

P0
REF_CLK
AUX_CLK
IPMC
Geog Addr[4:0]

Hardware Specifications

Form Factor:
- 3U OpenVPX card conforming to AV65-2010, 1" pitch and a payload profile of MOD3-PAY-2F2U-16.2.3-8
- Rugged conduction or air cooled
- Universal keying (unkeyed)

DSP0: Texas Instruments TCI6636/38 or 66AK2H12/14 KeystoneII DSP/ARM SoC
- 4 x 1.4 GHz ARM A15 cores
- 8 x 1.2 GHz C66x DSP cores
- Wireless accelerators (TCI parts only)
- 2 Gbytes x64 DDR3-1600 SDRAM
- 256 Mbytes x16 boot FLASH
- GigE to FPGA0, DSP1 and backplane
- HyperLink to DSP1 at up to 50 Gbaud
- 2x 5Gbaud PCIe to FPGA
- 2x AIF2 to FPGA
- 4x 5Gbaud SRIO to backplane
- 10 GigE XFI to backplane (TCI6638/66AK2H14 only)

DSP1: Texas Instruments TMS320C6678 Keystone DSP SoC
- 8 x 1.25GHz C66x DSP cores
- 2 Gbytes x64 DDR3-1333 SDRAM
- GigE and HyperLink to DSP0
- 4x 5Gbaud SRIO to backplane

FPGA: Xilinx Kintex-7™ K325T
- FFG676 package allows K160T to K410T
- 1 Gbyte x32 DDR3-1600 SDRAM
- 256 Mbytes x16 FLASH; allows storage of multiple FPGA configuration images
- 3x MGT, 32x LVDS, UART to backplane
- GigE to DSP0

Timing and sync:
- Timer, GPIO pins from FPGA to DSPs
- VPX REF_CLK and AUX_CLK inputs
- On-board PLL allows generation of high quality CPRI and RF clocks for DSP0, FPGA and backplane P2 connector

Debug: Connector for external debug breakout board with
- DSP and FPGA JTAG debug parts
- 2x RS232, to BMC and DSP0/FPGA0

Backplane I/O:
- Management and clocking to P0
- Two 4x SRIO links to P1 connector
- 3x FPGA MGT links to P1
- Dual Gigabit Ethernet links to P1
- 32x LDVS, 6x GPIO and UART to P2
- Powered from VS1 (+12V)

Environmental

Conduction cooled:
• Compliant to VITA 48.2 (REDI)
• Meets VITA 47 category ECC3
• Operating temp -40 to 70°C at wedgelocks
• Non-operating temp -50 to +100°C

Air cooled:
• Compliant to VITA 48.1 (REDI)
• Meets VITA 47 category EAC3
• Operating temp -40 to 70°C ambient
• Non-operating temp -50 to +100°C

Product Compliance:
• Power consumption: 30W typical
• 2014/30/EU EMC compliant
• 2011/65/EU RoHS compliant

Software/Firmware

ARM cores: Linux BSP and drivers, based on TI ARM Linux Multicore SDK with board specific additions and examples including FLASH upgrade

DSP cores: TI RTOS Kernel BSP and drivers, based on TI DSP Multicore SDK with board specific additions & examples

FPGA: Xilinx Vivado example/ default build which demonstrates board specific functionality and I/O, using Xilinx IP cores where appropriate.

OEM Development Services

Support and training; hardware customisation; software and FPGA development.

Lifecycle and Supply Assurance

Obsolescence management; guaranteed lifecycle; Escrow.

Licensing

Can be offered for very high volume projects.

All CommAgility developed software and firmware above is provided as source code to allow easy understanding and modification by customers, speeding application development.

BMC: Embedded software suite including I2C management interface, board control and FRU EEPROM data storage

LTE PHY: SmallCellPHY-TI is available fully integrated and tested, minimising customer development work.

CommAgility Ltd
Holywell Park, Ashby Road,
Loughborough, LE11 3AQ, UK

Tel: +44 (0)1509 228866
sales@commagility.com
www.commagility.com
@CommAgility