CommAgility Limited
Charnwood Building,
Holywell Park, Loughborough,
Leicestershire LE11 3AQ, UK.
Tel +44 (0) 1509 228866
www.commagility.com

Floating point multiprocessing with C66x DSPs from Texas Instruments

Paul Moakes, technical director, CommAgility (www.commagility.com)

Traditionally, DSPs have been either fixed- or floating-point. Recently, Texas Instruments Incorporated (TI) changed the game with processors based on its TMS320C66x core, which is capable of both fixed- and floating-point arithmetic.

New DSPs integrate fixed and floating

Fixed-point DSPs store and manipulate integers, while floating-point DSPs use a mantissa and exponent to represent rational numbers.

There are multiple factors which determine whether fixed- or floating-point is the right choice for a particular application, including cost, development time and performance.

Fixed-point DSPs have tended to be lower price, while floating-point DSPs have been easier for development while also providing higher accuracy and precision. This means that fixed-point DSPs have been used as high-volume, general-purpose processors, while floating-point DSPs have been chosen for specialized, processing-intensive tasks where dynamic range and precision are important.

According to TI, having a DSP core that integrates both fixed- and floating-point capability in the same DSP core enables a 'fundamental change' in the way algorithms for embedded systems are developed and deployed.

Put simply, up to now it was often necessary to implement algorithms on fixed-point DSPs because floating-point DSPs were not fast enough, but porting algorithms created with MATLAB or other floating point tools was slow and time-consuming.

TI's new C66x DSP core provides the floating-point capabilities needed to run such algorithms without sacrificing the speed of fixed-point. It achieved this by merging the C67x floating-point and the C64x fixed-point instruction sets into its C66x instruction set. This means that software can choose to execute floating-point or fixed-point commands on an instruction-by-instruction basis. The instruction set architecture is fully IEEE 754 compliant and supports both single- and double-precision floating point operations.

Applications for floating-point DSPs

There are many applications that can benefit from the improved speed and accuracy of floating-point DSPs as compared to fixed-point, and the increased affordability of DSPs based on the C66x core means that these benefits are more widely available than ever before.

For example, in wireless and radio systems, MIMO and beam-forming algorithms rely on matrix inversion techniques inherently susceptible to quantization and scaling errors associated with fixed-point processing. Using floating-point DSPs to implement these algorithms improves both

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the speed and the accuracy of the system, resulting in higher performance. The C66x DSP core runs MIMO and other key multi-antenna signal processing algorithms four times faster than the same algorithms running in fixed-point on the C64x DSP.

Radar, navigation and guidance systems process data that is acquired using arrays of sensors. To extract information on the location and movement of the target, the data must be processed as a set of linear equations. With a 1.25GHz floating-point engine like the C66x, a greater precision of output can be achieved, as well as a larger dynamic range, which means that these functions perform significantly better than with fixed-point DSPs.

Another application that benefits from the high degree of accuracy of floating-point is image processing. This can include image recognition, specifically medical imaging like ultrasound, as well as machine vision and industrial automation. In ultrasound, the greater precision given by the C66x enables imaging systems to achieve a much higher level of recognition and definition, thus improving the diagnostic process.

Similarly, audio processing and robot control are other applications that benefit from the higher precision and large dynamic range of floating-point.

The new TI DSPs – a closer look

TI offers multiple processors, based on its KeyStone architecture, that incorporate its C66x core. Let's take a closer look at two examples.

First, the TMS320C6678 is based on TI's KeyStone I architecture and includes eight C66x cores each running at up to 1.25GHz, enabling the equivalent of up to 10G cycles per second of DSP processing. Executing eight instructions per cycle allows (and having two-way single-instruction multiple data instruction supports) the headline figure of 160G floating-point operations per second (GFLOPS) by the device. The C66x core is fully backward compatible with the C6000 family of fixed- and floating-point DSPs.

The TMS320C6678 also provides a comprehensive set of I/O. This includes four lanes of low-latency Serial RapidIO (SRIO) 2.1 at 5Gbaud per lane full duplex and two lanes of PCIe Gen2, similarly at 5Gbaud per lane full duplex. An Ethernet MAC subsystem, two telecom serial ports, UART and I2C interfaces complete the conventional interfaces required by today's embedded devices.

In addition to the conventional I/O, the C6678 has a HyperLink interface. This high-speed, low pin count, point-to-point communication interface is designed to extend internal chip transactions between two KeyStone devices. Supporting rates of up to 12.5Gbaud per lane over four lanes, it can be used to aggregate the device resources of two C6678s DSPs, which can be viewed as a single 16-core system capable of 640GFLOPS.

The SmartReflex technology of TI's KeyStone devices can also decrease the dynamic power consumption while maintaining performance. Using a dedicated voltage regulator for each device, the device's core voltage is optimized based on the process corner of the device, maximizing the FLOPS per watt.

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Second, the new 66AK2H12 processor, based on TI's second generation KeyStone architecture (KeyStone II) combines quad ARM® Cortex™-A15 MPCore™ processors with eight TMS320C66x high-performance DSP cores. With core clocks raised to 1.4GHz, the 66AK2H12 provides up to 5.6GHz of ARM and 11.2GHz of DSP processing power. Coupled with security, packet processing and Ethernet switching engines, the device is a far cry from the ARM Cortex-A15 devices designed for consumer products.

The ARM Cortex-A15 MPCore processor combines leading processing capabilities with a very low power and performance ratio, multicore hardware-based cache coherency and broad industry software support. By integrating the ARM processors, there is no need in most applications for an additional high-end general purpose processor, which greatly reduces system cost and design complexity.

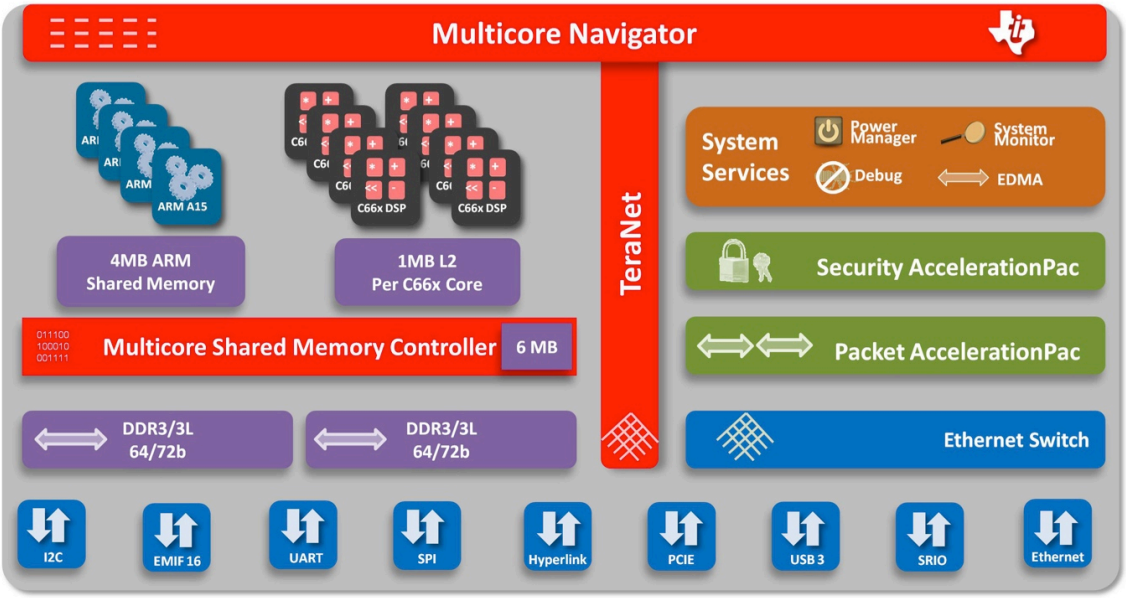

Figure 1: 66AK2H12 system on chip (courtesy of Texas Instruments)

With wide industry adoption of the ARM processors, developers can quickly and easily migrate existing software to the new KeyStone II-based devices. Full ARM-based Linux systems can be created, while offloading real-time processing to the high-performance C66x cores.

For more complex systems that need additional processing capacity, the 66AK2H12 has two HyperLink ports. These can be used to connect multiple KeyStone devices and thus add more C66x DSP cores, more ARM Cortex-A15 processors or both. HyperLink allows the devices to work in tandem transparently with tasks executed as if running on local devices.

The 66K2H12 is well suited to many applications that need high DSP performance and the control features of the ARM cores. For example, the mix of quad-core ARM and eight DSP cores in a fully-programmable SoC makes an ideal blend of processing power and flexibility on which to implement the highly complex codecs for high-quality video processing.

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Harnessing the power of the C66x DSP core

So how should all this DSP power be utilized?

CommAgility's aim has always been to be at the forefront of DSP technology, and supporting HyperLink and SmartReflex on our AMCs from the outset has allowed us to fully exploit the KeyStone devices. We consider the overall chip architecture with a view to multicore scalability and efficient power use.

Let's take the example of the CommAgility AMC-V7-2C6678, a high-performance signal processing AMC card with two 1.25GHz TMS320C6678 DSPs – giving a total of sixteen C66x cores. The two DSPs are linked with HyperLink, providing a connection at up to 50 Gbaud. They can access up to 2Gbyte x 64 DDR3-1333 SDRAM each.

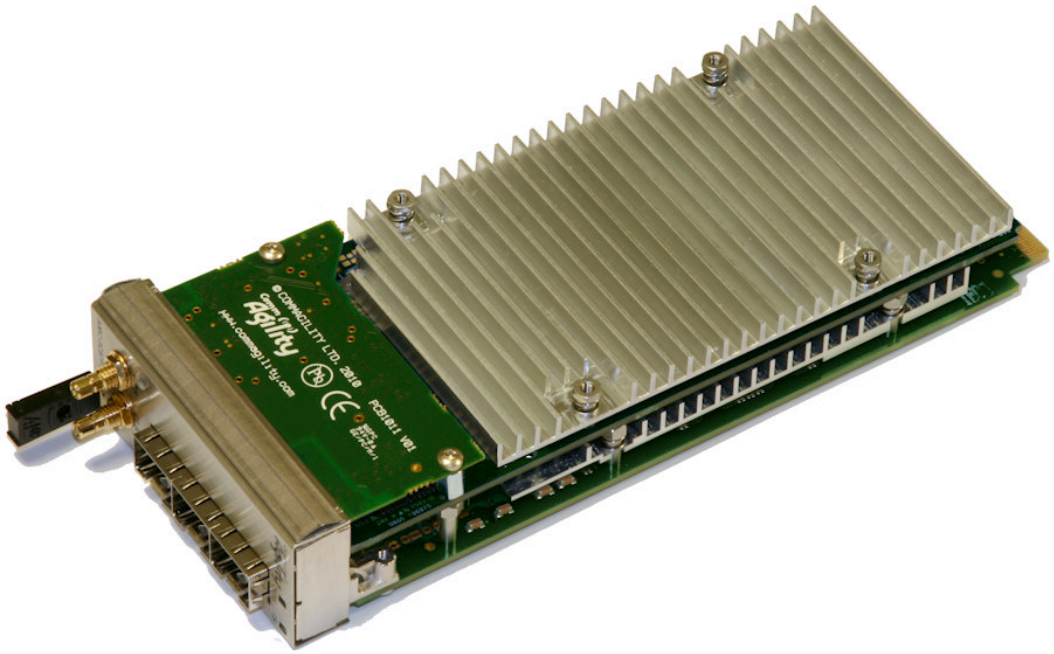

Figure 2: CommAgility AMC-V7-2C6678

Flexible, high bandwidth off-board communications are provided by Gen2 Serial RapidIO at up to 20Gbps per port. As standard, the board provides a single front panel SFP+ optical interface that links directly to the on-board Xilinx Virtex-7 FPGA, plus a mini-SAS connector linked to the SRIO switch. Should applications require timing and synchronization, this is achieved via the front panel or backplane clock I/O.

The AMC-V7-2C6678 is well-suited to a range of high performance DSP/FPGA processing applications, including telecoms infrastructure and image processing. By providing a high-performance FPGA, large shared memory and fast, flexible I/O, the horsepower of the TI DSPs can be harnessed and used effectively, while keeping power consumption, physical size and cost within tight limits.

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Another CommAgility board that uses the C66x DSPs is the new AMC-4C6678, which provides four TMS320C6678 devices running at 1.25GHz. This means there are a total of 32 cores, all closely linked, which provide a high level of performance for applications such as sensor processing, telecoms and image processing.

The AMC-4C6678 is a full-size, single width AMC, using an additional DSP mezzanine, and is suitable for MicroTCA systems. It features a wide range of connectivity to the backplane and front panel, including Gigabit Ethernet, PCI Express and SRIO. The PCI Express and Gigabit Ethernet connectivity use on-board switches for maximum flexibility and access to all DSPs on the card, while the SRIO link is directly connected to one DSP (shared using HyperLink) and then extends to the second DSP pair.

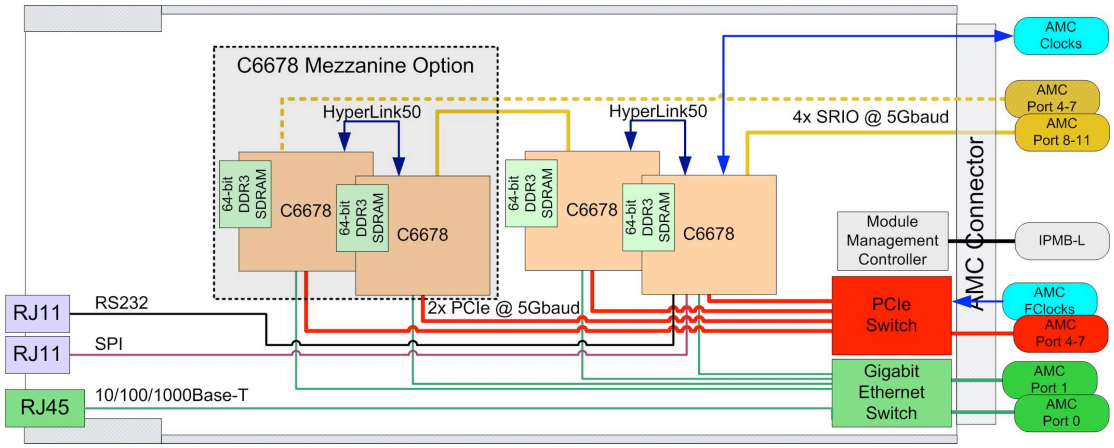

Figure 3: CommAgility AMC-4C6678 block diagram

VPX architectures

The VPX standard is defined by VITA as a platform that provides support for high-speed switched serial fabrics including Gigabit Ethernet, PCI Express, SRIO and InfiniBand. It retains the existing VME 6U and 3U form factor and includes support for PCI Mezzanine Card (PMC) and XMC mezzanines. Designed originally for mil/aero applications, VPX combines high performance with ruggedness.

CommAgility is working on architectures based on VPX that include TI's latest C66x DSPs. The first example takes advantage of TI's HyperLink to connect multiple devices and increase the ratio of real-time DSP processing power to general-purpose ARM-based platform management. Coupling TI's 66AK2H12 with a C6678 8-core DSP over HyperLink creates an arrangement that maximizes the MIPS/watt available.

This link between the 66AK2H12 and C6678 cores provides a platform with four ARM Cortex-A15 and 16 C66x DSP cores, which translates to 19600 Dhrystone MIPS and 198 FLOPS across the card.

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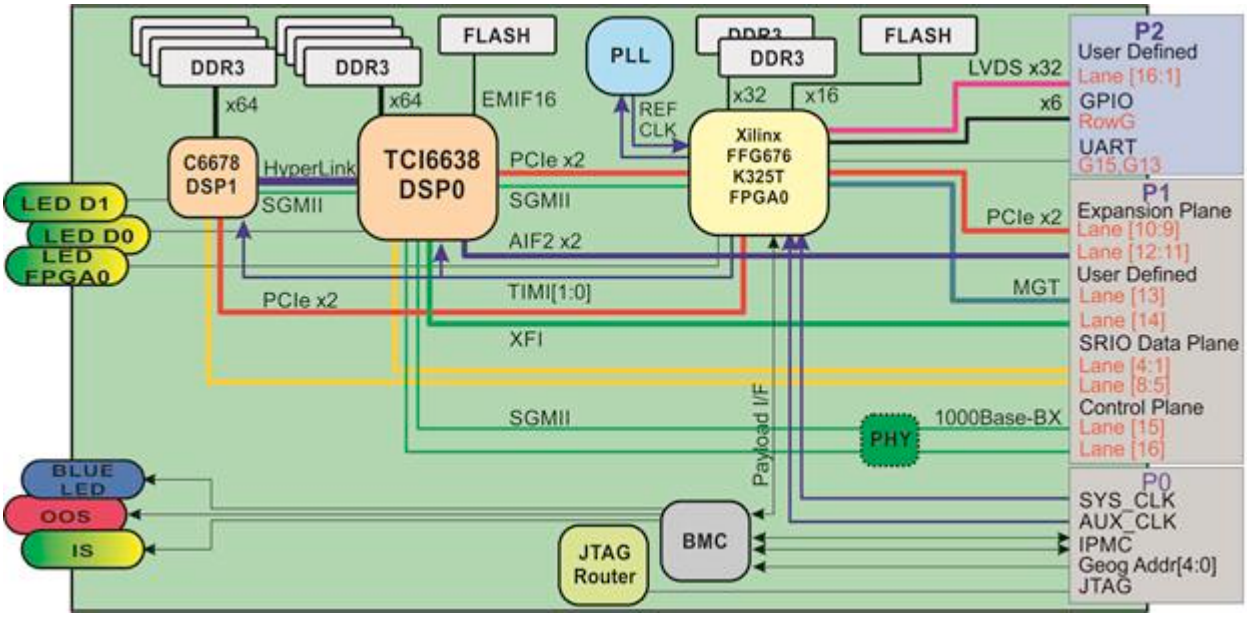

Figure 4: Proposed VPX board block diagram

The planned architecture will also include a Kintex™-7 FPGA from Xilinx, which provides high signal processing performance and low power consumption. The FPGA will enable the CommAgility boards to offer a high degree of I/O flexibility and will handle specialized co-processing tasks such as proprietary encryption, standards interworking and custom algorithm development.

The CommAgility VPX card is designed to the OpenVPX specification. With system-level design in mind, OpenVPX creates a framework of interoperability that allows customers to integrate cards and chassis from multiple vendors. This removes the need for card customization, reducing testing, cost and risk.

To provide flexible custom I/O, the architecture supports rear transition module (RTM) connections on P2. 32 LVDS pairs and 6 GPIO connections are provided from the Kintex-7 FPGA to the RTM site. This makes it easy for developers to deploy their own specialized IO or make use of a custom backplane to add support for a front IO module. For example, the RTM connection can be used to support ADC/DAC cards.

For infrastructure applications, high-performance networking interfaces are critical to deliver data to processors fast enough. The proposed architecture will include an on-chip five-port Ethernet switch, packet coprocessor and optional security coprocessor to provide carrier grade Ethernet throughput without the increase in processor loading that is normally associated with layer 2–4 processing, encryption and decryption. Other high-performance SerDes interfaces, including 20Gbps Serial RapidIO® (SRIO) and PCIe, deliver data to processors at infrastructure speeds, enabling the platform to handle tremendous data throughput.

For more information on Texas Instruments DSPs, see http://www.ti.com/lsds/ti/dsp/overview.page